

Form PTO-1449 (Modified) (Rev. 11/92)				U.S. Dept. of Commerce Patent and Trademark Office		ATTY. DOCKET NO. 254-094-CIP4/CIP-MB		SERIAL NO. 10/828,495	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))				APPLICANT Julian Partridge & James D. Wehrly, Jr.					
				FILING DATE 4/20/2004		GROUP 2822			
U.S. PATENT DOCUMENTS									
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	6,368,896B2	4/9/2002	Farnworth, Warren M. et al	438/113		4/23/1999			
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	Document Number	Date	Country	Class	Subclass	Translation			
						Yes	No		
TYT	58-96756(A)	06/08/1983	Japan			Partial			
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✓	EP 0 298 211 A#	01/11/1989	European			X			
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TYT	Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993								
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	"Design Techniques for Ball Grid Arrays," William R. Newberry, Xyntex Design Systems, Inc.								
EXAMINER	THANH TRAN			DATE CONSIDERED		12/30/04			
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Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No
TYT	62-230027(A)	10/08/1987	Japan			Partial
OTHER DOCUMENTS <i>(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)</i>						
TYT	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.					
TYT	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division					
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	Teresa Technologies, Inc. – Semiconductor Intellectual Property, Chip Scale Packaging – Website pages (3)					
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		(37 CFR 1.98(b))		FILING DATE	GROUP 2822
				4/20/2004	

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Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No

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TYT	Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
TYT	Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
TYT	"Vertically-Integrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

EXAMINER THANH TRAN DATE CONSIDERED 12/30/04

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